Quantum Random Access Memory

CPSC 4470/5470

Introduction to Quantum Computing

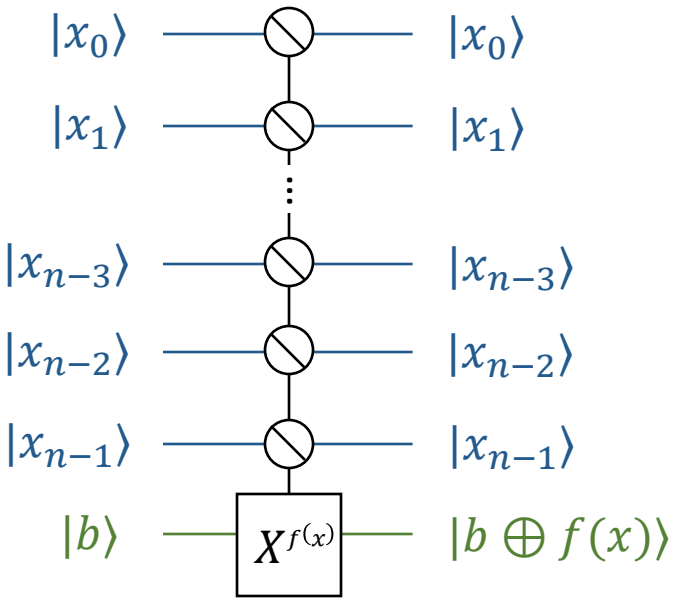
Instructor: Prof. **Yongshan Ding**

Computer Science, Applied Physics, Yale Quantum Institute

Implementing General-Purpose Oracles

Select Operator:

$$O_f = \prod_{x \in \{0,1\}^n} |x\rangle\langle x| \otimes X^{f(x)}$$



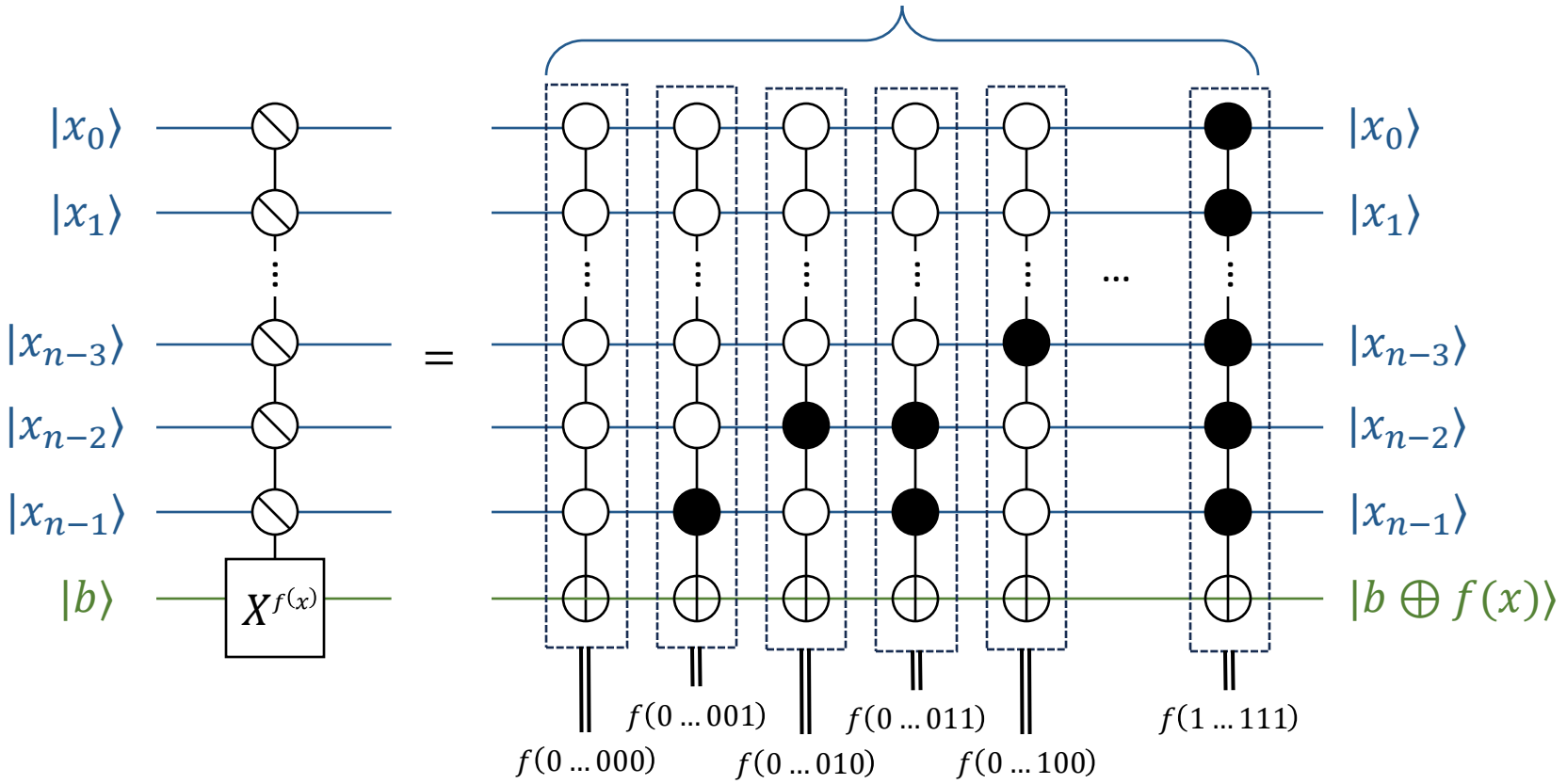
Implementations:

1. **Sequential Query Circuit:**
   - Gates: Toffoli, CX gates
   - Time: $O(N)$
   - Qubits: $\log N$ address qubits, 1 bus qubit, 1 ancilla qubit.

2. **Fanout QRAM:**
   - Gates: Fanout, cSWAP gates
   - Time: $O(\log N)$
   - Qubits: $\log N$ address qubits, 1 bus qubit, $O(N)$ ancilla qubits.

3. **Bucket-Brigade QRAM:**
   - Gates: cSWAP gates
   - Time: $O(\log N)$
   - Qubits: $\log N$ address qubits, 1 bus qubit, $O(N)$ ancilla qubits.

Sequential Query Circuit

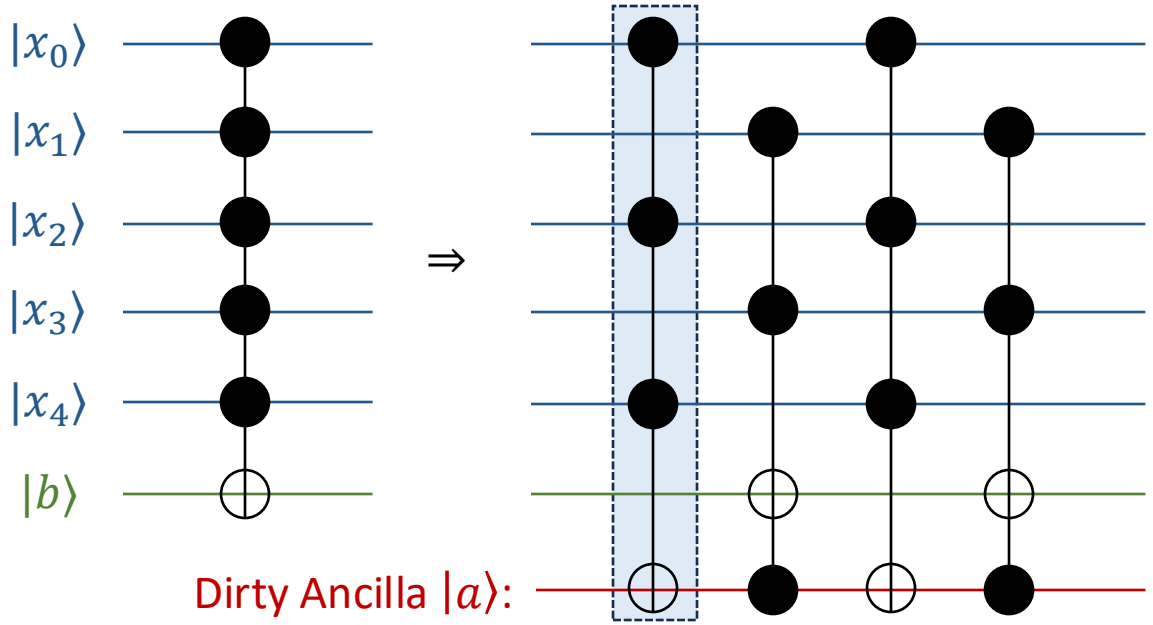


Implementing a Multi-Controlled-NOT Gate

Using Toffoli gates (acting on three qubits) and few ancillary qubits.

Example: $\Lambda_5(X)$ gate

Using multiple $\Lambda_3(X)$ gates?



$$\mathrm{AND}_5(x_0, x_1, x_2, x_3, x_4) = \mathrm{AND}_3(\mathrm{AND}_3(x_0, x_2, x_4), x_1, x_3)$$

What's the resulting state (including ancilla)?

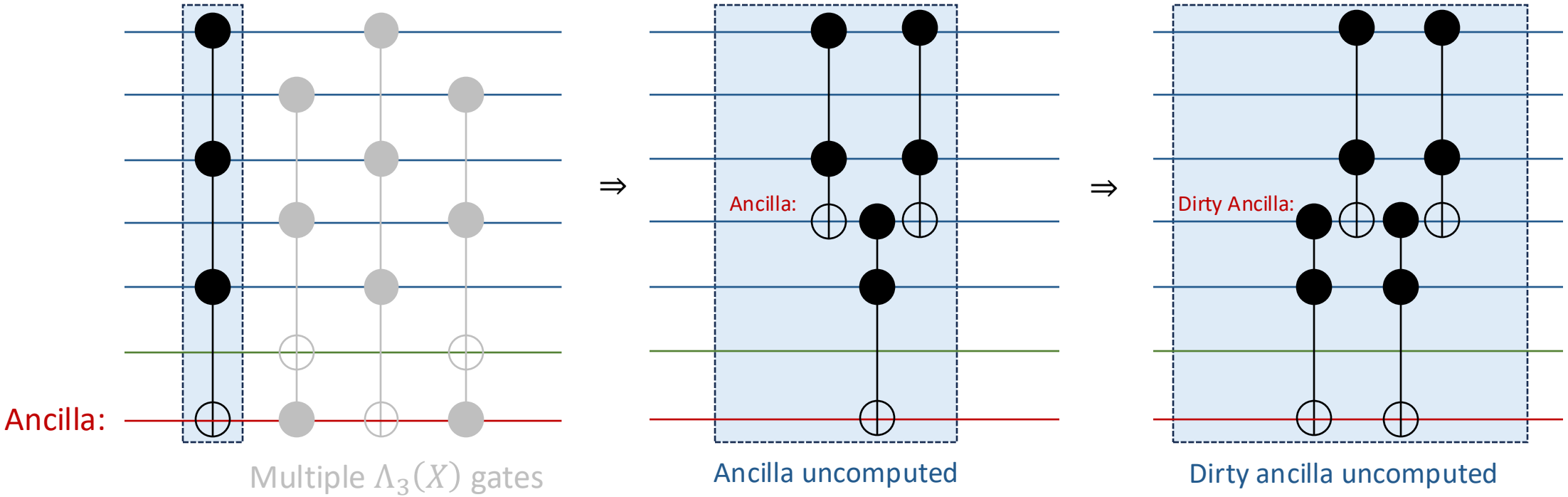
"Uncompute" to reset ancilla to initial state.

What if the initial ancilla state is unknown ("dirty")?

Write to output based on "toggling" ancilla state.

Implementing a Multi-Controlled-NOT Gate

Using Toffoli gates (acting on three qubits) and few ancillary qubits.



$$\mathrm{AND}_3(x_0, x_2, x_4) = \mathrm{AND}_2(\mathrm{AND}_2(x_0, x_2), x_4)$$

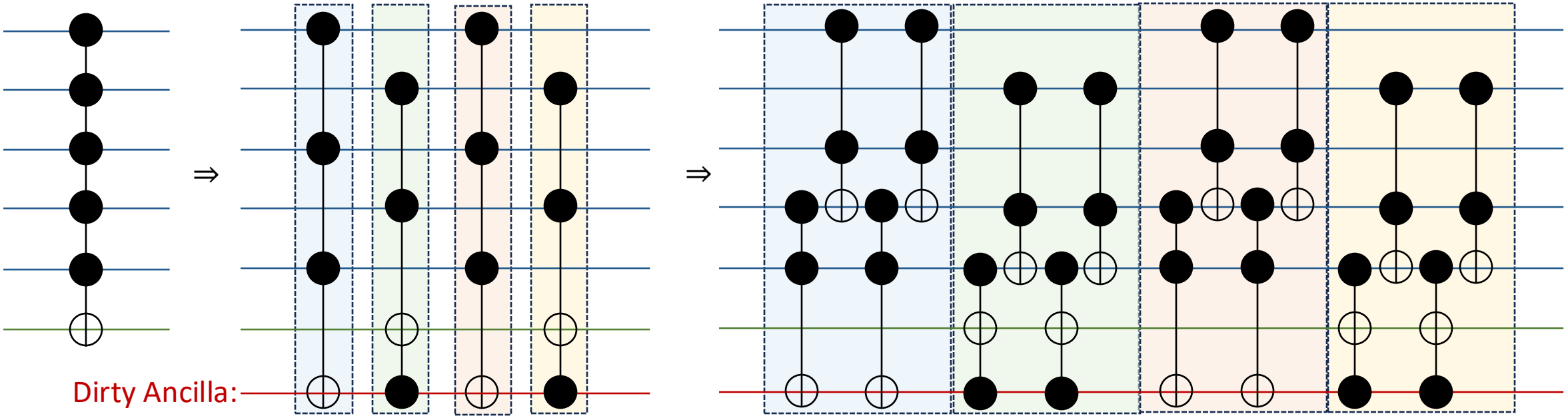
Implementing a Multi-Controlled-NOT Gate

Using Toffoli gates (acting on three qubits) and few ancillary qubits.

$\Lambda_5(X)$ gates

Multiple $\Lambda_3(X)$ gates

Multiple $\Lambda_2(X)$ (Toffoli) gates

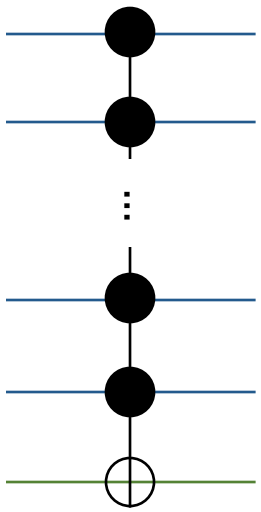


For $\Lambda_n(X)$ gate, we can implement using $\approx 16n$ Toffoli gates. **Total timesteps**: $O(n)$.

Implementing a Multi-Controlled-NOT Gate

Using Toffoli gates (acting on three qubits) and few ancillary qubits.

$\Lambda_n(X)$ gates



$\Rightarrow$

Implement AND_n using AND_2 gates and ancilla (qu)bits?

- We just saw: $O(n)$-size, $O(n)$-depth circuit with 1 ancilla.

$$\mathrm{AND}_n(x_0, \ldots, x_{n-1}) = \mathrm{AND}_{\lceil n/2 \rceil}\big(\underbrace{\mathrm{AND}_{\lceil n/2 \rceil}(x_{i:\mathrm{even}})}_{\mathrm{AND}_2(\ldots, \mathrm{AND}_2(\mathrm{AND}_2(x_0, x_2), x_4)}, x_{i:\mathrm{odd}}\big)$$

Can we do better?

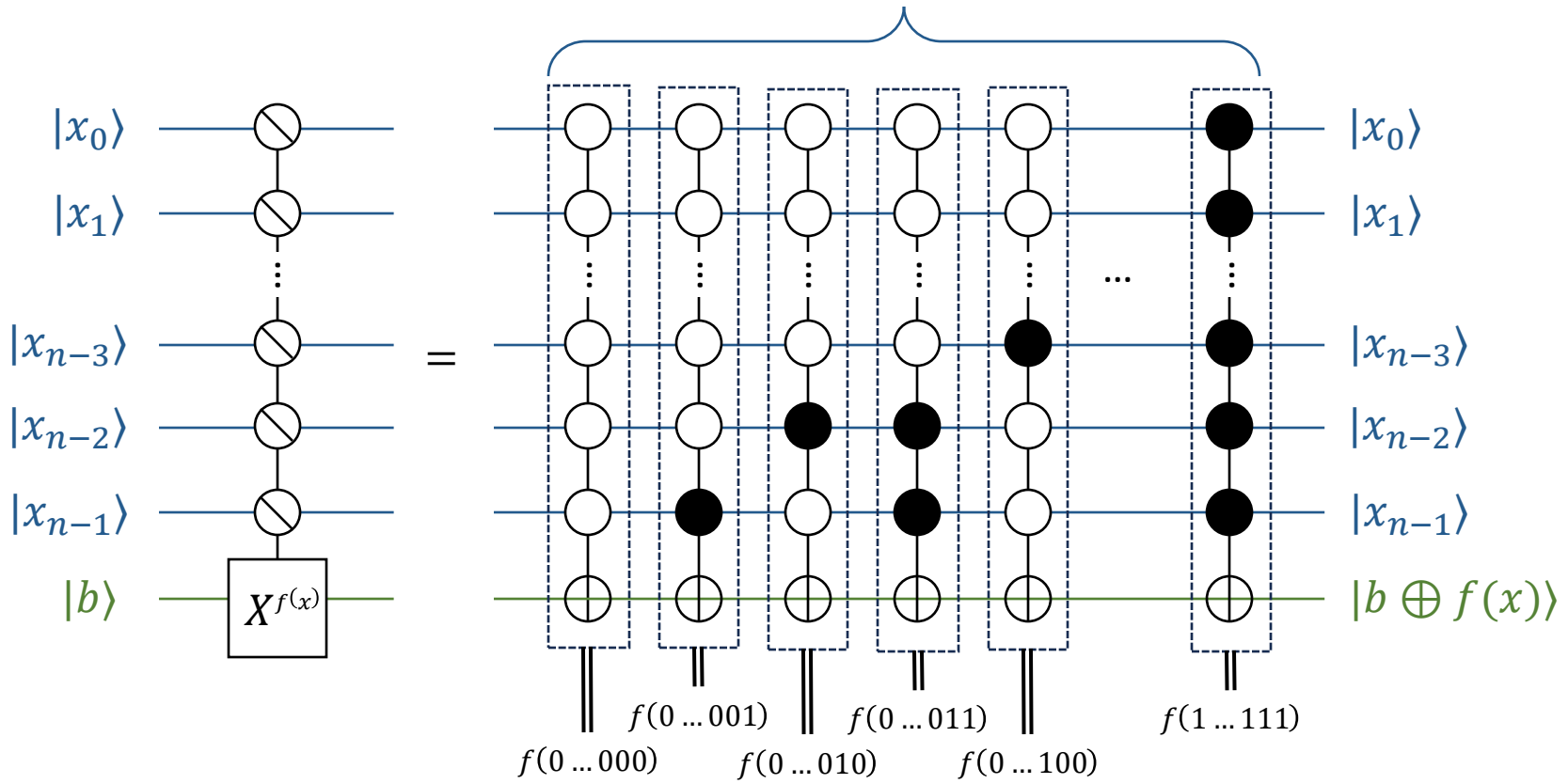
- **Logarithmic depth**: $O(n)$-size, $O(\log n)$-depth circuit with $O(n)$ ancilla.

  Binary tree of AND functions.

- **Constant depth**: $O(n)$-size, $O(1)$-depth **dynamic** circuit with $O(n \log n)$ ancilla.

  Dynamic circuit: mid-circuit measurement and feedforward.

Sequential Query Circuit



Each multi-controlled-NOT gate takes $O(n)$ time steps. What is the **total depth** for arbitrary $f(x)$?

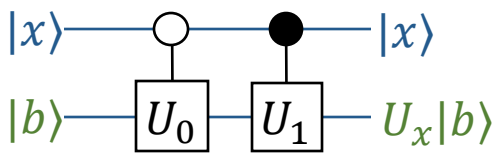
Quantum Multiplexer

Multiplexing Operator ($N = 2^n$):

$$\mathrm{MUX}_N = \prod_{x\in\{0,1\}^n} |x\rangle\langle x| \otimes U_x$$

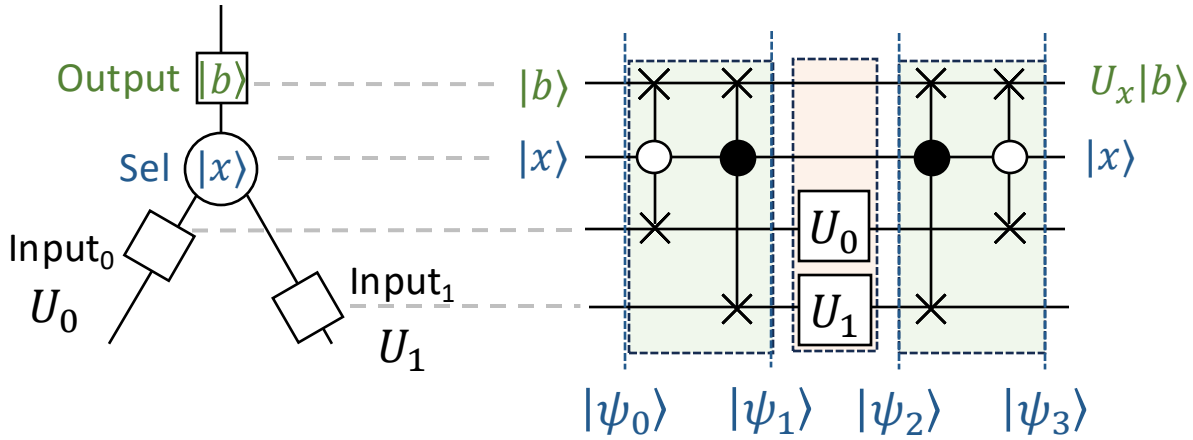
If select qubits are $|x\rangle$:
apply U_x to the output qubit.

Quantum Switch (MUX_2):

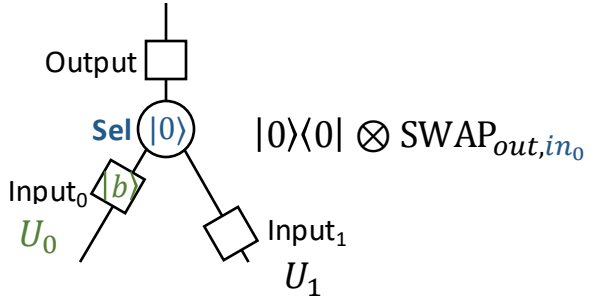


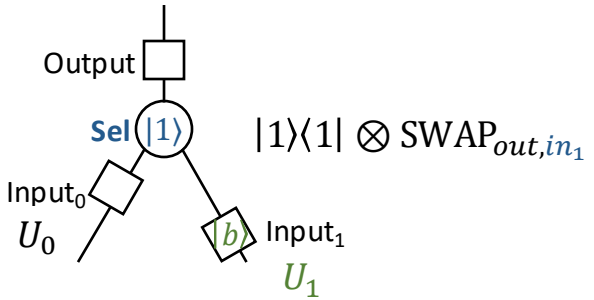
$$|0\rangle\langle 0| \otimes U_0 + |1\rangle\langle 1| \otimes U_1$$

Quantum Switch (implementing c-U's with cSWAP's and U's):



<u>Derive on board</u>: State of the quantum switch at each stage?





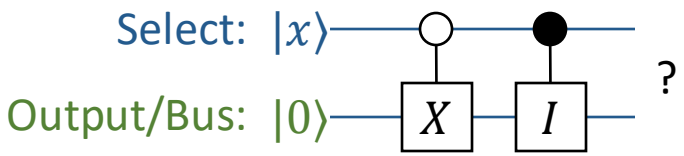
Quantum Oracle Using a Quantum Switch

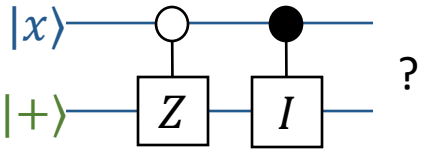
Multiplexing Operator ($N = 2^n$):

$$\mathrm{MUX}_N = \prod_{x\in\{0,1\}^n} |x\rangle\langle x| \otimes U_x$$

If select qubits are $|x\rangle$:
apply U_x to output qubit.

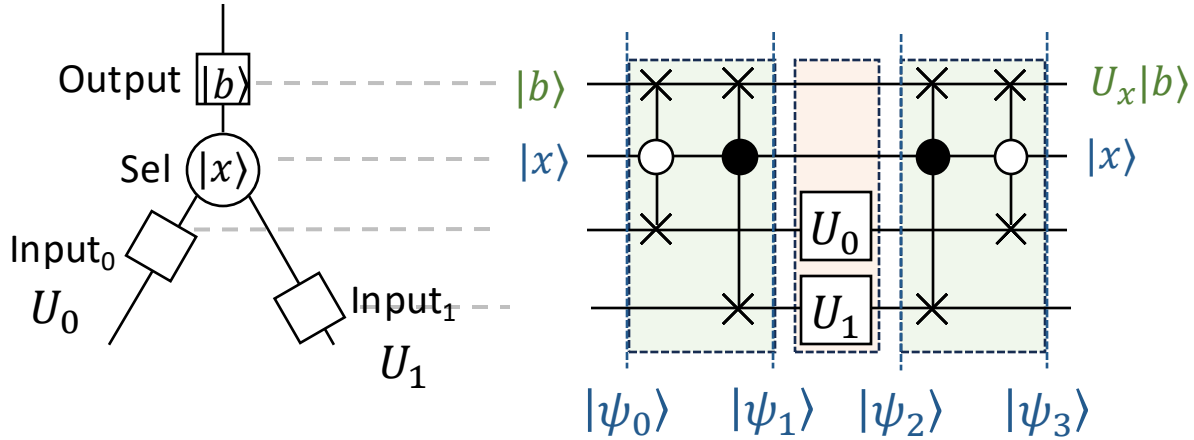
Bit oracle (for NOT function):



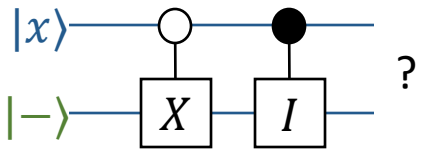


What initial state should we set for the ancilla?

Quantum Switch:



Phase oracle (for NOT function):



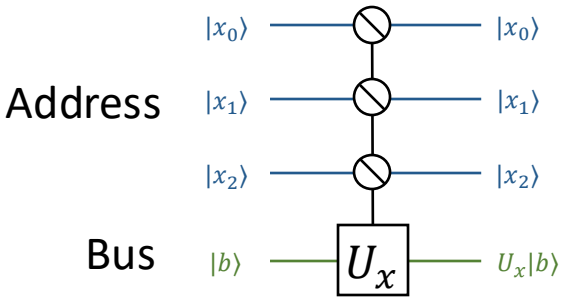
Quantum Multiplexer

Multiplexing Operator:

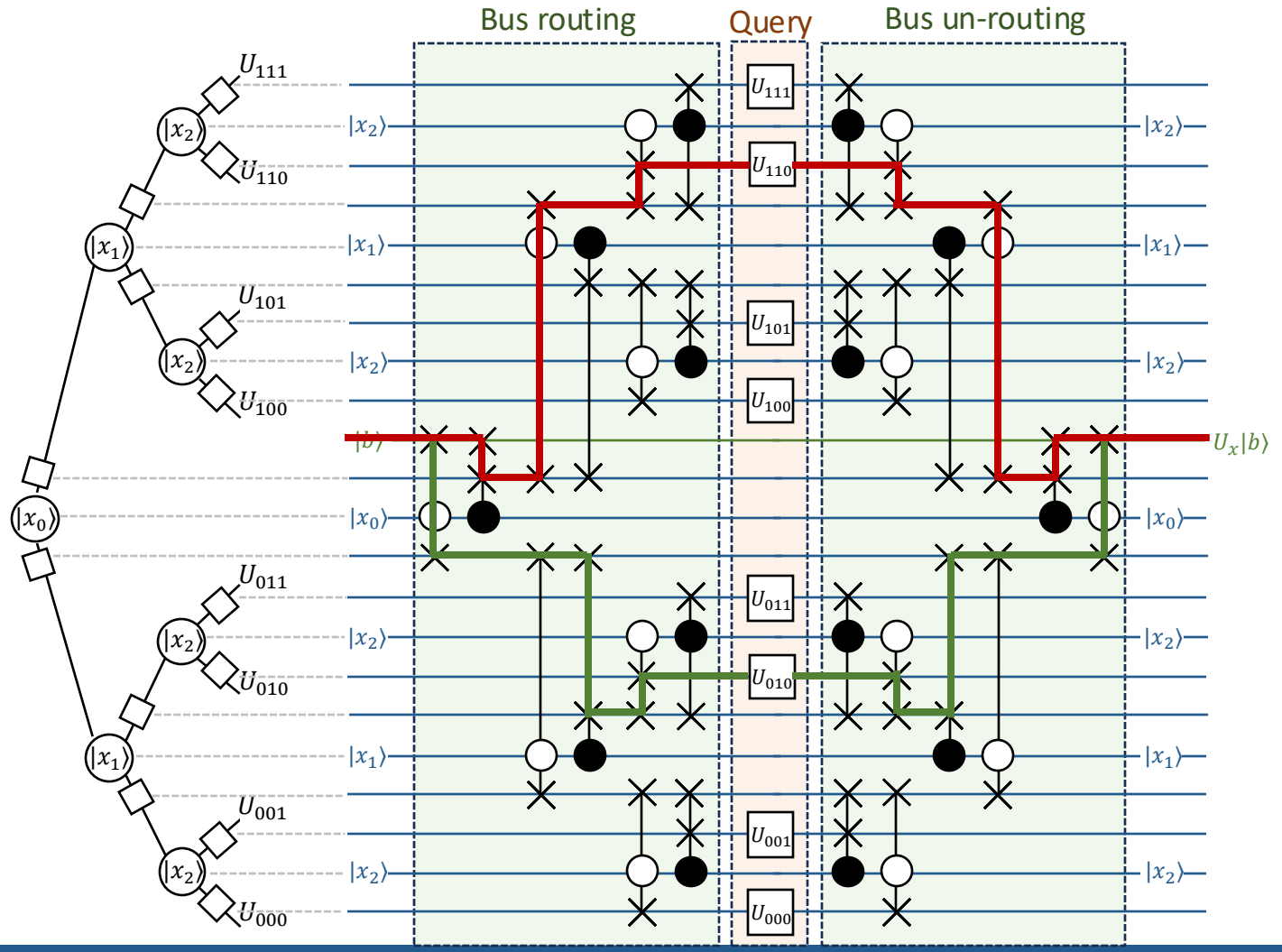
$$\mathrm{MUX}_N = \prod_{x\in\{0,1\}^n} |x\rangle\langle x| \otimes U_x$$

If select qubits are $|x\rangle$:
apply U_x to output qubit.

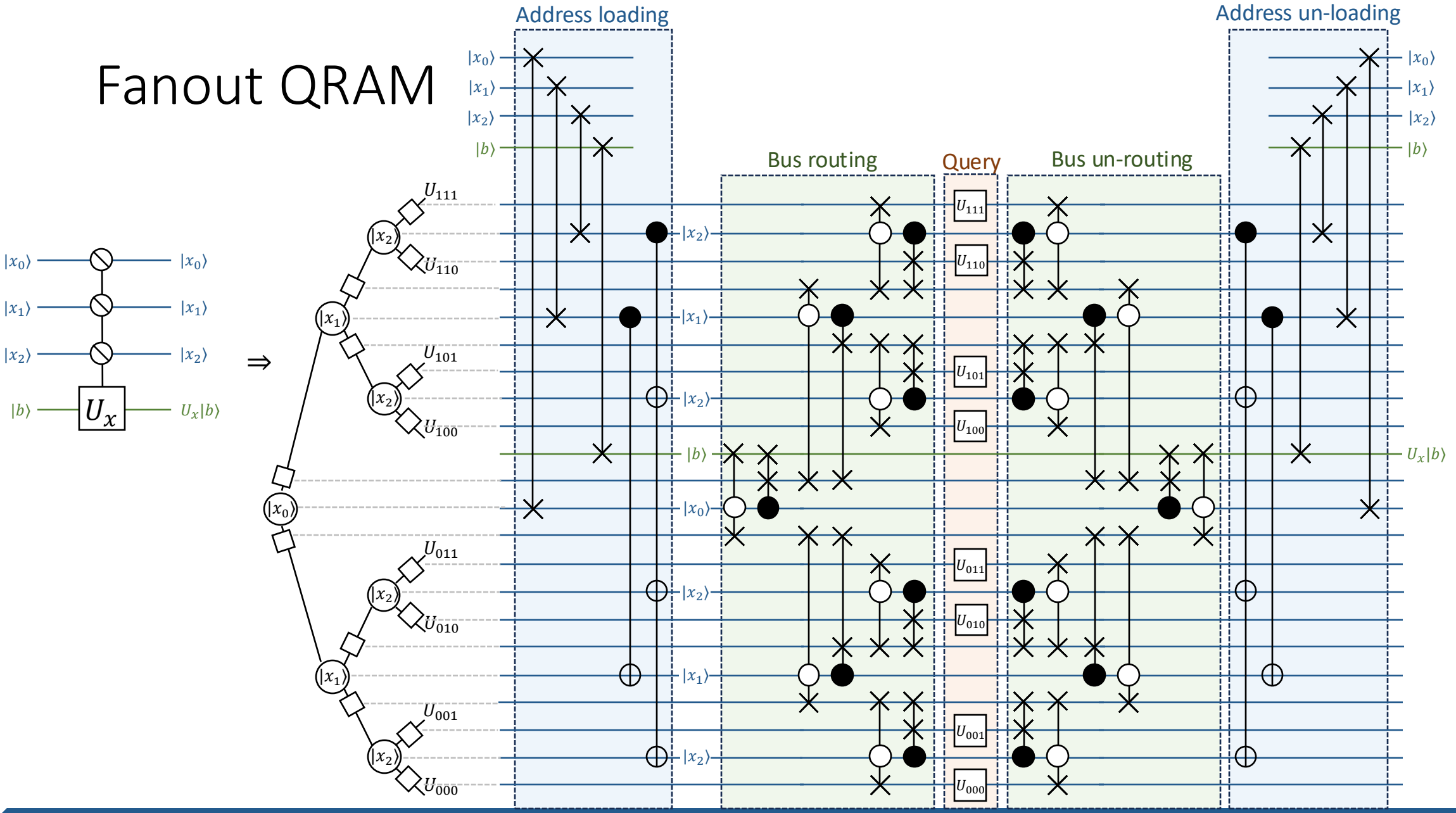
Example (MUX_8):



Quantum Multiplexer Tree Circuit:



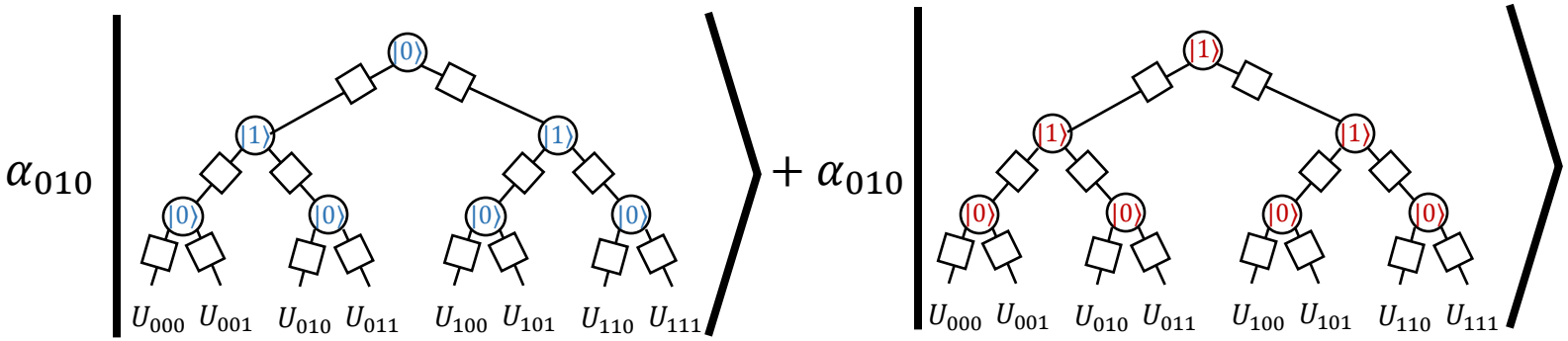
Fanout QRAM


Address loading
Bus routing
Query
Bus un-routing
Address un-loading
$|x_0\rangle$
$|x_1\rangle$
$|x_2\rangle$
$|b\rangle$
$U_x|b\rangle$
U_x
U_{111}
U_{110}
U_{101}
U_{100}
U_{011}
U_{010}
U_{001}
U_{000}

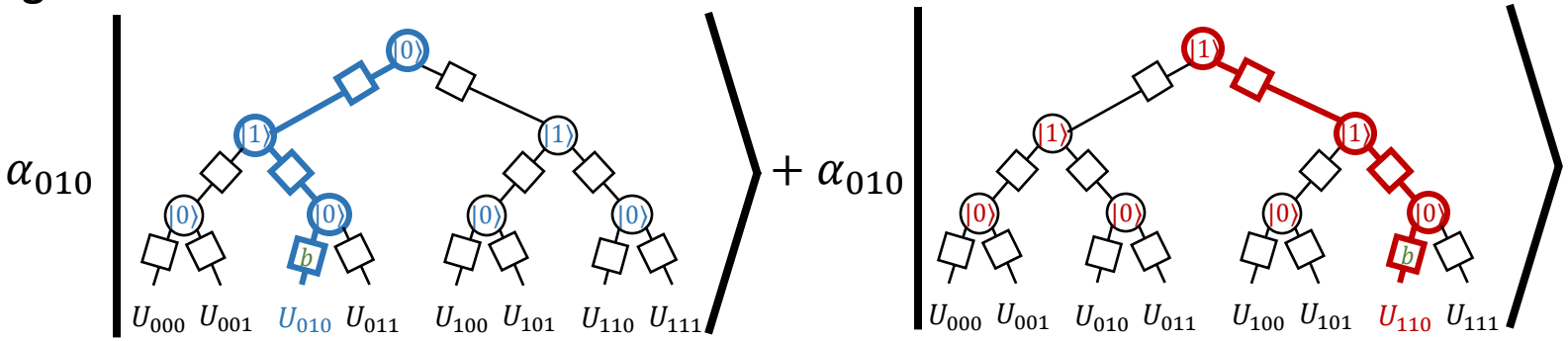
Fanout QRAM

Suppose address state is : $\alpha_{010}|010\rangle_a + \alpha_{010}|110\rangle_a$

After address loading:



After bus routing:

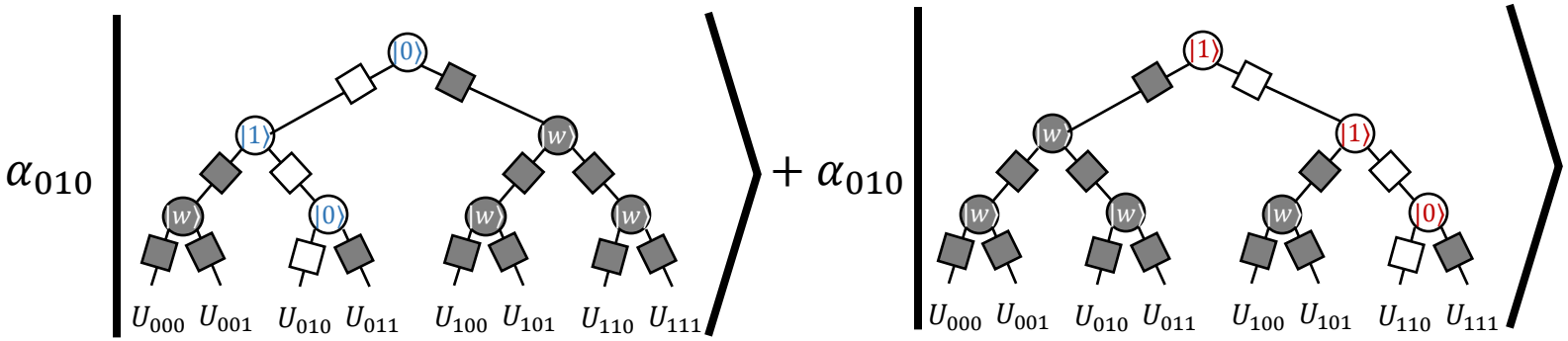


Bucket-Brigade QRAM

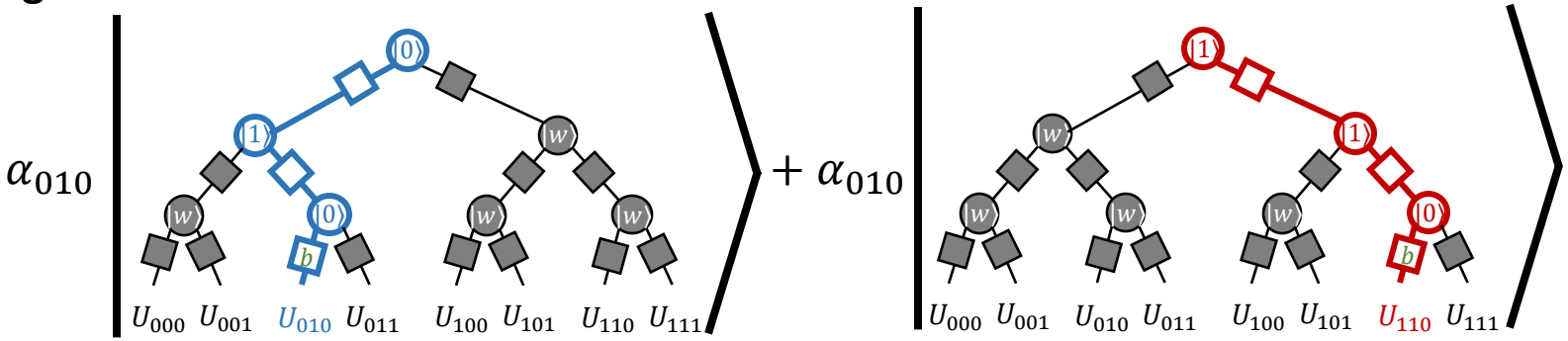
Suppose address state is : $\alpha_{010}|010\rangle_a + \alpha_{010}|110\rangle_a$

Introducing "wait" state: $|w\rangle$

After address loading:

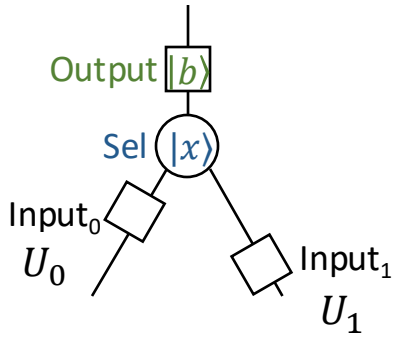


After bus routing:

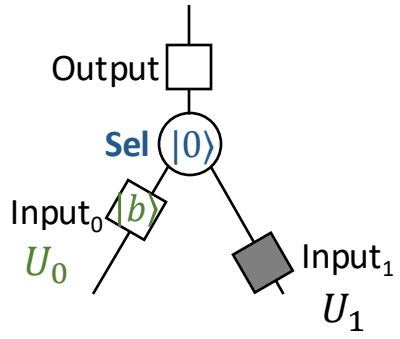


Quantum Switch on a Three-Level System

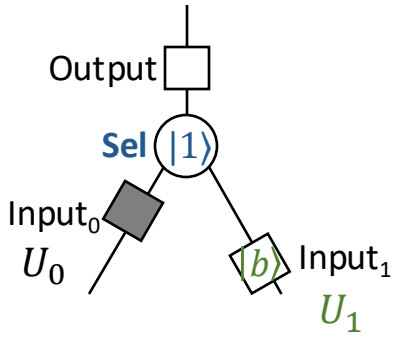
Quantum Switch (with wait):



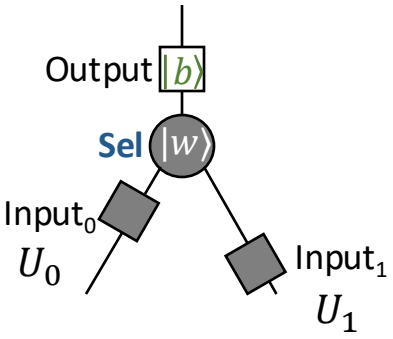
$x \in \{0,1,w\}$



$|0\rangle\langle 0| \otimes \mathrm{SWAP}_{out,in_0}$



$|1\rangle\langle 1| \otimes \mathrm{SWAP}_{out,in_1}$

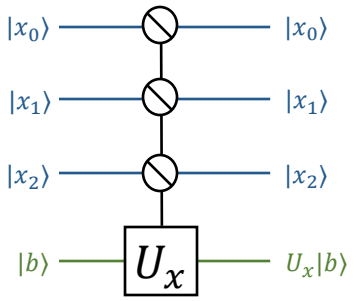


$|w\rangle\langle w| \otimes I$

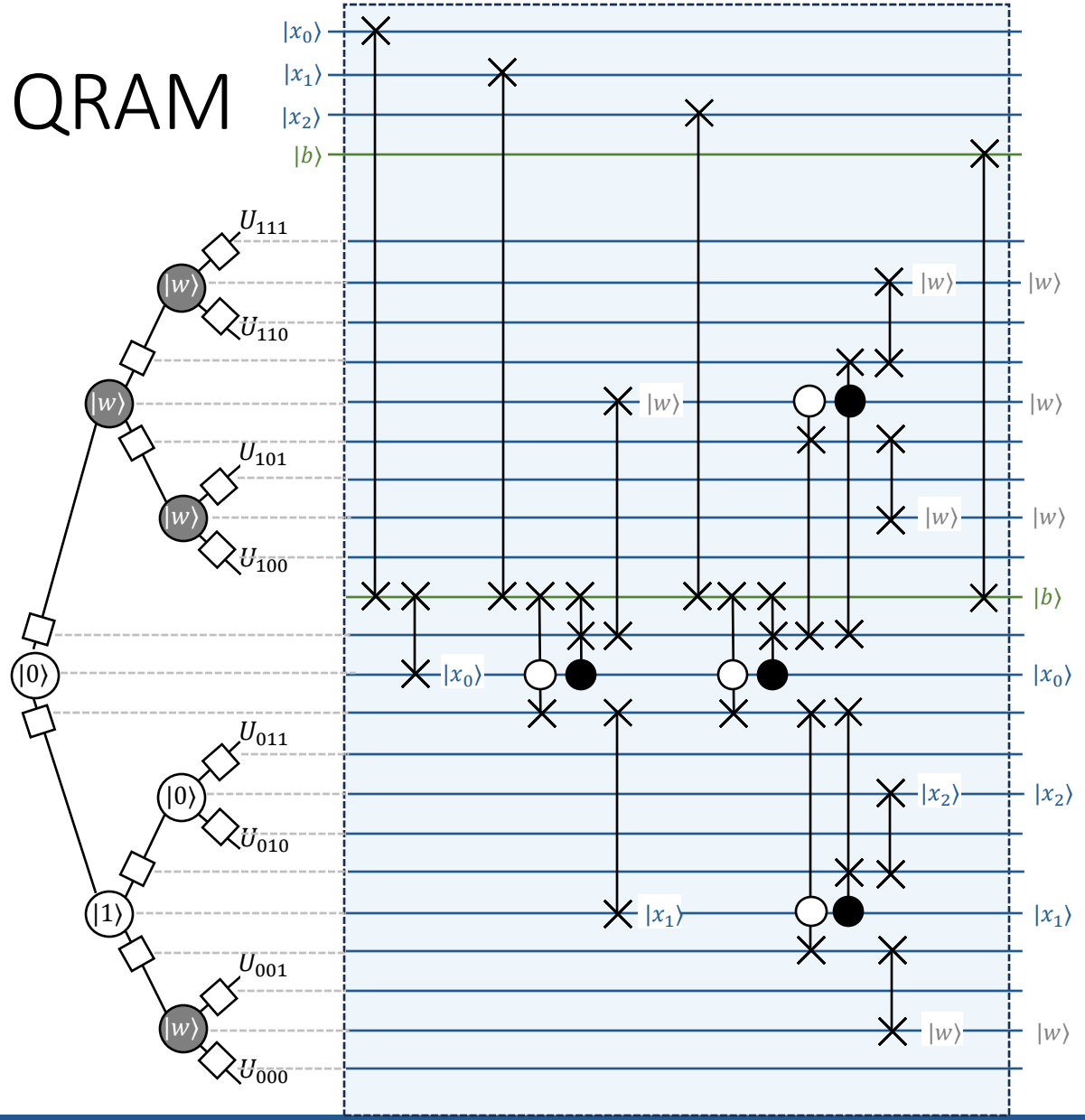
Qutrit: $\{|0\rangle, |1\rangle, |2\rangle\}$

2-Qubits: $\{|10\rangle, |01\rangle, |00\rangle\}$

Bucket-Brigade QRAM



$\Rightarrow$



Suppose $|x_0x_1x_2\rangle = |010\rangle$

<u>Derive on board</u>:

- Total qubits?
- Total depth?